CLAIMS

We claim:

1. A processor comprising:

a translation-lookaside-buffer (TLB);

a cache to provide temporary storage for a data block; and

a memory management unit to implement a first cache-coherency mechanism if the processor is in a first mode and to implement a second cache-coherency mechanism if the processor is in a second mode.

2. The processor of claim 1, wherein the TLB includes a plurality of entries, each entry including a virtual address tag, a physical address, and a memory attribute.

3. The processor of claim 2, wherein the first cache coherency mechanism snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected.

4. A computer system comprising:

an execution core;

a cache having a plurality of data entries;

a memory to store an operating system for the computer system; and

a memory management unit to manage data flow among the execution core, the cache and the memory, the memory controller to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system.

5. The computer system of claim 4, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing.